ABSTRACT

Methods, circuits, architectures, software and systems for error detection in transmitted data. The method generally includes the steps of (i) receiving digital information comprising data and non-data, the data comprising a plurality of data portions having a fixed length, (ii) removing at least one non-data portion; and (iii) if the data includes a remainder, adding a zero-pad vector to it to generate a zero-padded data portion, then checking the plurality of data portions and the zero-padded data portion for a transmission error. The circuit generally includes (a) a first logic circuit configured to detect non-data information; (b) a zero-fill circuit configured to replace at least a portion of the non-data information with a zero-pad vector; and (c) an error detection circuit configured to (i) detect a transmission error in data portions of the information and a zero-padded data portion of the information, the data portions and the zero-padded data portion having a fixed bit length, and (ii) combine the zero-pad vector with a remaining data portion of the information to form the zero-padded data portion. The architectures and/or systems generally include those that embody one or more of the inventive concepts disclosed herein, and the software is generally configured to implement steps in the present method. In the present invention, the data portions and the zero-padded data portion generally have the same bit length. This feature enables a single error detection circuit to detect an error on data of any unit length, thereby reducing the chip area dedicated to error detection, increasing the utilization efficiency of the circuitry on the chip, reducing power consumption, and (possibly) improving system performance.